What is claimed is:

1. A high voltage generation and regulation system comprising:

a charge pump generating a high voltage pump signal in response an enable signal and a medium voltage pump signal;

a pump loop regulator generating a plurality of high voltage signals having different voltage levels and the medium voltage pump signal in response to the high voltage pump signal; and

a nested loop regulator generating the enable signal in response to the high voltage pump signal being below a threshold voltage.

2. The high voltage generation and regulation system of claim 1 wherein the pump loop regulator comprises a comparator for controlling the voltage level of the plurality of high voltage signals in response to a control signal and a trimmable voltage divider for generating the control signal in response to said voltage level.

3. The high voltage generation and regulation system of claim 2 wherein the pump loop regulator includes a slew rate enhancement circuit to precharge the comparator output during power up.

4. The high voltage generation and regulation system of claim 1 wherein the charge pump generates an oscillator test signal.

5. The high voltage generation and regulation system of claim 1 wherein the charge pump includes a test port for monitoring an oscillator signal or receiving a test signal.

6. A charge pump system comprising:

a pump for generating a boosted voltage in response to at least two clock signals; and

an oscillator coupled to the pump for generating said at least two clock signals and including a ring oscillator, a multiplexer, and an output stage, the ring oscillator providing one of the at least one clock signals to the multiplexer and the output stage providing another one of the at least two clock signals to the multiplexer, the multiplexer outputting the two clock signals in

response to a first state of an enable signal and not outputting the two clock signals in response to a second state of the enable signal, the ring oscillator generating said one of the at least two clock signals independent of the enable signal.

7. A high voltage generation and regulation system comprising:

a charge pump comprising:

a pump for generating a boosted voltage signal in response to at least two clock signals and a feedback voltage signal; and

an oscillator coupled to the pump for generating said at least two clock signals and including a ring oscillator, an output stage, and a multiplexer, the ring oscillator providing one of the at least one clock signals to the multiplexer and the output stage providing another one of the at least two clock signals to the multiplexer, the multiplexer outputting the two clock signals in response to a first state of an enable signal and not outputting the two clock signals in response to a second state of the enable signal, the ring oscillator generating said one of the at least two clock signals independent of the enable signal; and

a loop regulator generating the feed back voltage signal in response to the boosted voltage signal.

8. A ring oscillator comprising:

a plurality of first inverters coupled in series with an output of one first inverter coupled to the input of another first inverter, one of said first inverters providing a first clock signal;

a plurality of first capacitors, each of said plurality of first capacitors being coupled to the output of a respective one of said plurality of first inverters;

a second inverter having an input coupled to the output of said one first inverter providing said first clock signal and having an output for providing a second clock signal; and

a second capacitor coupled to the output of the second inverter, the ratio of a capacitance of the second capacitor to a capacitance of the first capacitors being such to adjust the phase between the first and second clock signals to a pre-selected value.

9. A high voltage generation and regulation system comprising:

a charge pump comprising:

a pump for generating a boosted voltage signal in response to at least two clock signals and a feedback voltage signal; and

a plurality of first inverters coupled in series with an output of one first inverter coupled to the input of another first inverter, one of said first inverters providing a first clock signal;

a plurality of first capacitors, each of said plurality of first capacitors being coupled to the output of a respective one of said plurality of first inverters;

a second inverter having an input coupled to the output of said one first inverter providing said first clock signal and having an output for providing a second clock signal; and

a second capacitor coupled to the output of the second inverter, the ratio of a capacitance of the second capacitor to a capacitance of the first capacitors being such to adjust the phase between the first and second clock signals to a pre-selected value; and

a loop regulator generating the feedback voltage signal in response to the boosted voltage signal.

10. A ring oscillator comprising:

a plurality of first inverters coupled in series with an output of one first inverter coupled to the input of another first inverter, each of said plurality of inverters providing a first inverted signal having characteristics dependent on an applied first bias current, one of said first inverters providing a first clock signal;

a plurality of first capacitors, each of said plurality of first capacitors being coupled to the output of a respective one of said plurality of first inverters;

a second inverter having an input coupled to the output of said one first inverter providing said first clock signal and having an output for providing a second clock signal having characteristics dependent on an applied second bias current, the ratio of first bias current to the second bias current being such to adjust the phase between the first and second clock signals to a pre-selected value; and

a second capacitor coupled to the output of the second inverter, the capacitance of each of the plurality of first capacitors being equal to the capacitance of the second capacitor.

11. A high voltage generation and regulation system comprising:

a charge pump comprising:

a pump for generating a boosted voltage signal in response to at least two clock signals and a feedback voltage signal,

a plurality of first inverters coupled in series with an output of one first inverter coupled to the input of another first inverter, each of said plurality of inverters providing a first inverted signal having characteristics dependent on an applied first bias current, one of said first inverters providing a first clock signal,

a plurality of first capacitors, each of said plurality of first capacitors being coupled to the output of a respective one of said plurality of first inverters,

a second inverter having an input coupled to the output of said one first inverter providing said first clock signal and having an output for providing a second clock signal having characteristics dependent on an applied second bias current, the ratio of first bias current to the second bias current being such to adjust the phase between the first and second clock signals to a pre-selected value,

a second capacitor coupled to the output of the second inverter, the capacitance of each of the plurality of first capacitors being equal to the capacitance of the second capacitor; and

a loop regulator generating the feed back voltage signal in response to the boosted voltage signal.

12. A charge pump comprising:

a plurality of voltage boost stages coupled in series, each of the voltage boost stages generating an output signal having a voltage level higher than an input voltage applied thereto, and each comprising a first transistor including a first terminal coupled to receive said input voltage and including a second terminal for providing said output signal, and further comprising a powerup assist diode to charge the input voltage applied to the voltage boost stage coupled to the output signal.

13. The charge pump of claim 13 wherein each voltage boost stage comprises a circuit to forward cancel the threshold voltage of the first transistor.

14. The charge pump of claim 13 wherein said circuit comprises a cancellation transistor including a first terminal coupled to the first terminal of the first transistor, including a second

terminal spaced apart from said first terminal of the cancellation transistor with a channel therebetween and coupled to a gate of the first transistor and including a gate coupled to the first terminal of the second transistor.

15. The charge pump of claim 14 wherein said circuit further comprises a third transistor to backward cancel the threshold voltage of the first transistor.

16. The charge pump of claim 15 wherein the third transistor includes a first terminal coupled to the first terminal of the first transistor, and including a second terminal spaced apart from said second terminal with a channel therebetween and coupled to a gate of the first transistor and including a gate for controlling current in said channel and coupled to the second terminal of the first transistor.

17. The charge pump of claim 12 wherein each boost stage comprises a circuit to backward cancel the threshold voltage of the first transistor.

18. The charge pump of claim 17 wherein the circuit comprises a second transistor including a first terminal coupled to the first terminal of the first transistor, including a second terminal spaced apart from the first terminal of the second transistor with a channel therebetween and coupled to the gate of the first transistor and including a gate for controlling current in said channel and coupled to the second terminal of the first transistor.

19. The charge pump of claim 12 wherein each voltage boost stage comprises a cancellation transistor coupled to the first terminal to substantially cancel a threshold voltage of the first transistor in response to the output signal.

20. The charge pump of claim 12 wherein at least one of the plurality of voltage boost stages includes a high voltage self-biasing circuit to precharge the output signal before application of said input voltage.

21. The charge pump of claim 20 wherein the high voltage self-biasing circuit comprises a second transistor including a first terminal coupled to a supply voltage terminal, including a

second terminal spaced apart from said first terminal with a channel therebetween, and including a gate for controlling current in said channel and coupled to said first terminal, and comprises a third transistor including a first terminal coupled to the second terminal of the second transistor, including a second terminal spaced apart from said first terminal with a channel therebetween and coupled to the output signal, and including a gate for controlling current in said channel and coupled to a medium voltage terminal.

22. The charge pump of claim 21 wherein a medium voltage applied to the medium voltage terminal has a voltage level between a voltage level of a supply voltage applied to the supply voltage terminal and a voltage level of the output signal of the last voltage boost stage.

23. A charge pump comprising:

a plurality of voltage boost stages coupled in series, each of the voltage boost stages generating an output signal having a voltage level higher than an input voltage applied thereto, and each comprising a first transistor including a first terminal coupled to receive said input voltage and including a second terminal for providing said output signal, and further comprising a first circuit for canceling the forward threshold voltage of the first transistor and a second circuit for canceling the backward threshold voltage of the first transistor.

24. A charge pump comprising:

a plurality of voltage boost stages coupled in series, each of the voltage boost stages generating an output signal having a voltage level higher than an input voltage applied thereto, and each comprising a first transistor including a first terminal coupled to received said input voltage and including a second terminal for providing said output signal, at least one of the plurality of voltage boost stages includes a high voltage self-biasing circuit to precharge the output signal for application of said input voltage.

25. The charge pump of claim 24 wherein the high voltage self-biasing circuit comprises a second transistor including a first terminal coupled to a supply voltage terminal, including a second terminal spaced apart from said terminal with a channel therebetween and including a gate for controlling current in said channel and coupled to said first terminal, and comprises a third transistor including a first terminal coupled to the second terminal of the second transistor,

including a second terminal spaced apart from said first terminal with a channel therebetween and coupled to the output signal, and including a gate for controlling current in said channel and coupled to the median voltage terminal.

26. The charge pump of claim 25 wherein a median voltage applied to the median voltage terminal has a voltage level between a voltage level of a supply voltage applied to the supplied voltage terminal and a voltage level of the output signal of the last voltage boost stage.

27. A high voltage generation and regulation system comprising:

a charge pump generating a boosted voltage signal in response to at least two clock signals and a feedback voltage signal comprising:

a plurality of voltage boost stages coupled in series, each of the voltage boost stages generating an output signal having a voltage level higher than an input voltage applied thereto, and each comprising a first transistor including a first terminal coupled to receive said input voltage and including a second terminal for providing said output signal, and further comprising a powerup assist diode to charge the input voltage applied to the voltage boost stage coupled to the output signal, and

an oscillator coupled to the plurality of voltage boost stages for generating said at least two clock signals; and

a loop regulator generating the feed back voltage signal in response to the boosted voltage signal.

28. The high voltage generation and regulation system of claim 27 wherein each voltage boost stage comprises a cancellation transistor coupled to the first terminal to substantially cancel a threshold voltage of the first transistor in response to the output signal.

29. The high voltage generation and regulation system of claim 27 wherein at least one of the plurality of voltage boost stages includes a high voltage self-biasing circuit to precharge the output signal before application of said input voltage.

30. The high voltage generation and regulation system of claim 29 wherein the high voltage self-biasing circuit comprises a second transistor including a first terminal coupled to a supply

voltage terminal, including a second terminal spaced apart from said terminal with a channel therebetween, and including a gate for controlling current in said channel and coupled to said first terminal, and comprises a third transistor including a first terminal coupled to the second terminal of the second transistor, including a second terminal spaced apart from said first terminal with a channel therebetween and coupled to the output signal, and including a gate for controlling current in said channel and coupled to a medium voltage terminal.

31. The high voltage generation and regulation system of claim 30 wherein a medium voltage applied to the medium voltage terminal has a voltage level between a voltage level of a supply voltage applied to the supply voltage terminal and a voltage level of the output signal of the last voltage boost stage.

32. A regulator circuit comprising:

a voltage regulator providing a regulated voltage signal in response to an input voltage signal and a control signal;

a comparator coupled to the voltage regulator to generate the control signal in response to the regulated voltage signal; and

a slew rate enhancement circuit coupled to an output of the comparator to boost the control signal in the event the regulated voltage signal has a voltage level less than a threshold voltage.

33. The regulator circuit of claim 32 wherein the slew rate enhancement circuit comprises a source follower.

34. The regulator circuit of claim 33 wherein the slew rate enhancement circuit further comprises a voltage divider to generate a divided voltage signal in response to the input voltage signal and wherein the source follower provides said boost of the control signal in response to said divided voltage signal.

35. The regulator circuit of claim 34 wherein a level of said boost of the control signal is adjustable.

36. The regulator circuit of claim 32 wherein a level of said boost of the control signal is adjustable.

37. The regulator circuit of claim 32 wherein the threshold voltage is below a peak voltage of the regulated voltage signal.

38. The regulator circuit of claim 34 further comprising a self-biasing circuit to precharge the output terminal during power up.

39. The regulator circuit of claim 33 further comprising a self-biasing circuit to precharge the output terminal during power-up.

40. The regulator circuit of claim 32 further comprising a self-biasing circuit to precharge the output terminal during power-up.

41. A high voltage generation and regulation system comprising:

a charge pump for generating a voltage signal in response to at least two clock signals and a feedback signal;

a loop regulator generating the feedback voltage signal in response to the boosted voltage signal, the loop regulator comprising;

a voltage regulator providing a regulated voltage signal in response to an input voltage signal and a control signal;

a comparator coupled to the voltage regulator to generate the control signal in response to the regulated voltage signal; and

a slew rate enhancement circuit coupled to an output of the comparator to boost the control signal in the event the regulated voltage signal has a voltage level less than a threshold voltage.

42. The high voltage generation and regulation system of claim 41 wherein the slew rate enhancement circuit comprises a source follower.

43. The high voltage generation and regulation system of claim 42 wherein the slew rate enhancement circuit further comprises a voltage regulator to generate a divided voltage signal in response to the input voltage signal and wherein the source follower provides said boost of the control signal in response to said divided voltage signal.

44. The high voltage generation and regulation system of claim 43 wherein the slew rate enhancement circuit compensates for the output of the comparator.

45. The high voltage generation and regulation system of claim 41 wherein the slew rate enhancement circuit provides compensation for the output of the comparator.

46. The high voltage generation and regulation system of claim 41 wherein the threshold voltage is below a peak voltage of the regulated voltage signal.

47. The high voltage generation and regulation system of claim 46 wherein the threshold voltage is no greater than 100 millivolts below the peak voltage of the regulated voltage signal.

48. The high voltage generation and regulation system of claim 41 further comprising a self-biasing circuit to precharge the output terminal during power up.

49. A high voltage series regulator comprising:

a high voltage input terminal;

an output terminal;

a first transistor including a first terminal coupled to the high voltage input terminal, including a second terminal spaced apart from said first terminal with a channel therebetween, and including a gate for controlling current in said channel;

a second transistor including a first terminal coupled to the second terminal of the first transistor, including a second terminal coupled to the output terminal to provide an output voltage thereto and spaced apart from said first terminal with a channel therebetween, and including a gate for controlling current in said channel and coupled to the gate of the first transistor;

a feedback voltage generator coupled to the output terminal to generate a feedback voltage in response to the output voltage; and

a comparator having a first input coupled to the feedback voltage generator, a second input coupled to a reference voltage terminal and an output coupled to the gates of the first and second transistors.

50. The high voltage series regulator of claim 49 wherein the feedback voltage generator is a voltage divider.

51. The high voltage series regulator of claim 50 wherein the voltage divider comprises:

a plurality of third transistors coupled in series between the output terminal and a ground terminal, each of the plurality of third transistors being diode connected, one of the plurality of third transistors providing the feedback voltage.

52. The high voltage series regulator of claim 51 wherein the voltage divider further comprises a fourth transistor coupled between another one of the plurality of third transistors and ground to float a voltage of a terminal of said another one of the plurality of third transistor in response to a power down signal.

53. The high voltage series regulator of claim 52 wherein at least one of the plurality of third transistors is selectively shunted.

54. The high voltage series regulator of claim 51 wherein at least one of the plurality of third transistors is selectively shunted.

55. The high voltage series regulator of claim 50 wherein the voltage divider comprises a plurality of p-channel diodes coupled in series between the output terminal and a second terminal at a voltage less than the voltage of the output terminal.

56. The high voltage series regulator of claim 50 further comprising a trimming circuit to selectively select ones of said plurality of third transistors.

57. The high voltage series regulator of claim 56 wherein the trimming circuit comprises a plurality of fourth transistors coupled in series, each of the plurality of fourth transistors including first and second terminal coupled to respective first and second terminals of a corresponding one of the plurality of third transistors and including a gate coupled to a respective select signal to change the feedback voltage.

58. The high voltage series regulator of claim 49 further comprising a filter coupled between the high voltage input terminal and the comparator.

59. The high voltage series regulator of claim 58 wherein the filter is a resistor-capacitor filter.

60. The high voltage series regulator of claim 49 further comprising:

a third transistor including a first terminal coupled to a supply voltage, including a second terminal spaced apart from said first terminal with a channel therebetween, and including a gate coupled to said first terminal for controlling current in said channel, and

a fourth transistor including a first terminal coupled to the second terminal of the third transistor, including a second terminal coupled to the output terminal and spaced apart from said first terminal with a channel therebetween, and including a gate for controlling current in said channel in response to a control voltage applied thereto, the control voltage being a function of the voltage on the output terminal.

61. The high voltage series regulator of claim 60 wherein the voltage of the control voltage biases the fourth transistor to prevent breakdown of the fourth transistor.

62. A high voltage generation and regulation system comprising:

a charge pump for generating a voltage signal in response to at least two clock signals and a feedback signal;

a loop regulator generating the feedback voltage signal in response to the boosted voltage signal, the loop regulator comprising;

a high voltage input terminal;

an output terminal;

a first transistor including a first terminal coupled to the high voltage input terminal, including a second terminal spaced apart from said first terminal with a channel therebetween, and including a gate for controlling current in said channel;

a second transistor including a first terminal coupled to the second terminal of the first transistor, including a second terminal coupled to the output terminal to provide an output voltage thereto and spaced apart from said first terminal with a channel therebetween, and including a gate for controlling current in said channel and coupled to the gate of the first transistor;

a feedback voltage generator coupled to the output terminal to generate a feedback voltage in response to the output voltage; and

a comparator having a first input coupled to the feedback voltage generator, a second input coupled to a reference voltage terminal and an output coupled to the gates of the first and second transistors.

63. The high voltage generation and regulation system of claim 62 wherein the feedback voltage generator is a voltage divider.

64. The high voltage generation and regulation system of claim 63 wherein the voltage divider comprises:

a plurality of third transistors coupled in series between the output terminal and a ground terminal, each of the plurality of third transistors being diode connected, one of the plurality of third transistors providing the feedback voltage.

65. The high voltage generation and regulation system of claim 64 wherein the voltage divider further comprises a fourth transistor coupled between another one of the plurality of third transistors and ground to float a voltage of a terminal of said another one of the plurality of third transistor in response to a power down signal.

66. The high voltage generation and regulation system of claim 65 wherein at least one of the plurality of third transistors is selectively shunted.

67. The high voltage generation and regulation system of claim 64 wherein at least one of the plurality of third transistors is selectively shunted.

68. The high voltage generation and regulation system of claim 63 wherein the voltage divider comprises a plurality of p-channel diodes coupled in series between the output terminal and a second terminal at a voltage less than the voltage of the output terminal.

69. The high voltage generation and regulation system of claim 63 further comprising a trimming circuit to selectively select ones of said plurality of third transistors.

70. The high voltage generation and regulation system of claim 69 wherein the trimming circuit comprises a plurality of fourth transistors coupled in series, each of the plurality of fourth transistors including first and second terminal coupled to respective first and second terminals of a corresponding one of the plurality of third transistors and including a gate coupled to a respective select signal to change the feedback voltage.

71. The high voltage generation and regulation system of claim 62 further comprising a filter coupled between the high voltage input terminal and the comparator.

72. The high voltage generation and regulation system of claim 71 wherein the filter is a resistor-capacitor filter.

73. The high voltage generation and regulation system of claim 62 further comprising:

a third transistor including a first terminal coupled to a supply voltage, including a second terminal spaced apart from said first terminal with a channel therebetween, and including a gate coupled to said first terminal for controlling current in said channel, and

a fourth transistor including a first terminal coupled to the second terminal of the third transistor, including a second terminal coupled to the output terminal and spaced apart from said first terminal with a channel therebetween, and including a gate for controlling current in said channel in response to a control voltage applied thereto, the control voltage being a function of the voltage on the output terminal.

74. The high voltage generation and regulation system of claim 73 wherein the voltage of the control voltage biases the fourth transistor to prevent breakdown of the fourth transistor.

75. A nested loop regulator comprising:

a voltage divider generating a divided voltage signal in response to a high voltage output signal from a charge pump; and

a comparator having a first input coupled to the voltage divider, having a second input for receiving a reference voltage, and having an output for generating an enable signal to enable a charge pump in response to the divided voltage signal being below the reference voltage.

76. The nested loop regulator of claim 75 further compressing a capacitor coupled to an input of the voltage divider to filter said high voltage output signal.

77. The nested loop regulator of claim 75, wherein the voltage divider comprises:

a plurality of transistors, each transistor including a first terminal, a second terminal spaced apart from said first terminal with a channel therebetween, and a gate for controlling current in said channel, the first terminal of a first one of said plurality of transistors being coupled to receive the charge pump high voltage output signal, the gate of a second one of said plurality of transistors being coupled to ground and the second terminal of said second one of said plurality of transistors being coupled to ground, the first terminal of each of the other ones of said transistors being coupled to the second terminal of another one of said plurality of transistors to form a cascode arrangement.

78. The nested loop regulator of claim 77 wherein the voltage divider further comprises another transistor including a first terminal and second terminals, a channel between said first and second terminals, and a gate for controlling current in said channel and coupled to a power enable signal, the first and second terminals of said another transistor being coupled between the second terminal of said second one of the plurality of transistors and ground.

79. A voltage regulation system comprising:

a charge pump having a first input for receiving an enable signal, having a second input for receiving a regulated voltage signal, and having an output for providing a pump voltage signal in response to the regulated voltage signal and the enable signal;

a pump regulator coupled to the charge pump for providing the regulated voltage signal in response to the pump voltage signal; and

a nested loop regulator having an input coupled to the output of the charge pump and having an output for generating the enable signal in response to the pump voltage signal being below a threshold voltage.

80. The voltage regulation system of claim 79 wherein the nested loop regulator comprises:

a voltage divider generating a divided voltage signal in response to the pump voltage signal; and

a comparator having a first input coupled to the voltage divider, having a second input for receiving a reference voltage having a threshold voltage level, and having an output for providing the enable signal in response to the divided voltage signal being below the reference voltage.

81. The voltage regulation system of claim 79 wherein the voltage divider comprises:

a plurality of transistors, each transistor including a first terminal, a second terminal spaced apart from said first terminal with a channel therebetween, and a gate for controlling current in said channel, the first terminal of a first one of said plurality of transistors being coupled to receive the charge pump high voltage output signal, the gate of a second one of said plurality of transistors being coupled to ground and the second terminal of said second one of said plurality of transistors being coupled to ground, the first terminal of each of the other ones of said transistors being coupled to the second terminal of another one of said plurality of transistors to form a cascode arrangement

82. The voltage regulation system of claim 81 wherein the voltage divider further comprises another transistor including a first terminal and second terminals, a channel between said first and second terminals, and a gate for controlling current in said channel and coupled to a power enable signal, the first and second terminals of said another transistor being coupled between the second terminal of said second one of the plurality of transistors and ground.